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Substitute for form 1449A	/P10			Application Number	10/759559	
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STATE	MENT BY AF	PLIC	ANT	First Named Inventor	Rodney E. Hooker	
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Sheet	1	of	11_	Attorney Docket Number	CNTR.2057	

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RD		GB2307319	05-21-1997	Han Heung Kim		

Examiner	/Ryan Dare/	Date	06/25/2006
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RD		GB2260429	04-14-1993	Kagan et al.		
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Examiner Cite C	Document Number	Publication Date	Name of Patentee or	Pages, Columns, Lines, Where	
Initials*	No.1	Number-Kind Code ^{2(# known)}	MM-DD-YYYY	Applicant of Cited Document	Relevant Passages or Relevant Figures Appear
RD		3401376	09-10-1968	Barnes et al.	
I		3810117	05-07-1974	Robert A. Healey	
		6038643	03-14-2000	Tremblay et al.	
		6671196	12-30-2003	Jan Civlin	
		6425055	07-23-2002	Sager et al.	
		5500950	03-19-1996	Becker et al.	
		5751990	05-12-1998	Krolak et al.	
<u> </u>		5956752	09-21-1999	Gregory S. Mathews	
V		6275903	08-14-2001	Koppala et al.	
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			_	Group Art Unit	2188
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Sheet	1	of	1	Attorney Docket Number	CNTR.2057

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RD		5980467	09-28-1999	Mahalingaiah et al.	
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INFORMATION DISCLOSURE	Filing Date	1/16/2004	
STATEMENT BY APPLICANT	First Named Inventor	Rodney E. Hooker	
	Group Art Unit	2188	
(use as many sheets as necessary	Examiner Name	Mano Padmadabahn	
Sheet 1 of 1	Attorney Docket Number	CNTR.2057	

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initials*	No.	Number-Kind Code ^{2(d known)}	MM-DD-YYYY	Applicant of Cited Document	Relevant Passages or Relevant Figure: Appear
RD		2002144061	10-03-2002	. Faanes et al.	
RD		2004133886	07-08-2004	Youfeng Wu	
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RD		5930820	07-27-1999	Thomas W. Lynch				
RD .		B151661	11-21-2000	Adams et al.	,			
RD		20040186959	09-23-2004	Takuji Kawamoto				
RD ·		6415380	07-02-2002	Toshinori Sato	·			
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RD	AA	GB2307319	05-21-1997	Han Heung Kim		↓_				
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RD	ВА	"Dual On-Chip Instruction Cache Organization in High Speed Processors." IBM Technical Disclosuro Bulletin. IBM Corp. New York, US. Volume 37, No. 12, December 1994. pages 213-214.	
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RD	AA	5043870		Ditzel et al	08/27/1991	1
RD	AB	5953741		Evoy et al	09/14/1999	
RD	AC	6009499		Sailendra Koppala	12/28/1999	
RD	AD	6532531		O'Connor et al	03/11/2003	_
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First Named Inventor	Rodney E. Hooker			
Group Art Unit				
Examiner Name				
Attorney Docket Number	CNTR.2057			

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RD	AA	(in the file SCreport.pdf): Implementing a Stack Cache; Hensath, Morton, Sjodin; obtained from http://www.owlnet.rice.edu/~elec525/projects/SCreport.pdf ; accessed on 8-13-2003.				
RD	AB	(in the file JavaStack Cache.doc); Design Issues — Stack Cache; obtained from http://murray.newcastle.edu.au/users/students/1999/c9510422/design1.html; http://murray.newcastle.edu.au/users/students/1999/c9510422/design2.html; http://murray.newcastle.edu.au/users/students/1999/c9510422/design3.html; http://murray.newcastle.edu.au/users/students/1999/c9510422/design4.html; http://murray.newcastle.edu.au/users/students/1999/c9510422/architecture.html; accessed on 12-02-2003.				
RD	AC	(in the fine AMD Hammer micro architecture.pdf): AMD's Hammer micro architecture; http://chip-architect.com/news/hammer.jpg ; accessed on 08-29-2002.				

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